REMARKS

Claims 1-10 are pending in this application, with claims 1, 6, 7, 8 and 9 being independent.

Applicant acknowledges with appreciation the Examiner's allowance of claims 9 and 10 and the Examiner's indication that claim 8 is directed to allowable subject matter.

The title and the specification have been amended in response to the Examiner's objections. These amendments are believed to address all of the Examiner's concerns. No new matter has been added.

With respect to the Examiner's objection to claim 8, applicant disagrees that "a" should precede "circular buffer control logic".

Claims 1 and 2 have been rejected as being anticipated by Davis. Applicant requests reconsideration and withdrawal of this rejection because Davis does not describe or suggest "instruction fetch logic that simultaneously fetches two instructions and routes them to respective pipelines;" as recited in claim 1 (emphasis added). Instead of describing simultaneous fetching, Davis describes fetching two instructions during the same process cycle. In particular, Davis notes, at col. 5, lines 30-33 (emphasis added), "[f]etching and decoding of both processor (A) instructions and processor (B) instructions alternately occur within the same process cycle so that the same silicon can be used for both pipelines." Thus, instead of fetching the instructions simultaneously, Davis fetches them in an alternating manner. This is further illustrated in Fig. 5 of Davis, which shows the decode/fetch for processor (A) occurring during the first two clock phases of a process cycle and the decode/fetch for processor (B) occurring during the second two clock phases of the process cycle.

Claim 7, which had been rejected as being anticipated by Gatherer, has been amended to recite hardware configured to execute a complex multiply instruction on complex numbers stored in the register pair, where each complex number includes a real portion and an imaginary portion. Applicant requests reconsideration and withdrawal of the rejection of claim 7 because Gatherer does not describe or suggest hardware configured to execute a complex multiply instruction.

Claims 3-5, which depend from claim 1, have been rejected as being unpatentable in view of Davis. Applicant requests reconsideration and withdrawal of this rejection because, as discussed above with respect to claim 1, Davis fails to describe or suggest the subject matter of claim 1.

Claim 6 has been rejected as being unpatentable in view of Bloomgren. Applicant requests reconsideration and withdrawal of this rejection because Bloomgren does not describe or suggest integrating subopcodes into an established instruction set, or doing so in the manner recited in claim 6. In particular, Bloomgren does not describe or suggest "an instruction decoder that identifies a relocatable opcode to designate 64 subopcodes;" or "a subopcode detector that decodes subopcodes if the instruction decoder identifies the relocatable opcode[,]" as recited in claim 6. Instead, as noted by the Examiner, Bloomgren is directed to an emulator that breaks down an unsupported CISC instruction into a series of RISC instructions. Thus, rather than decoding subopcodes (i.e., selecting a subopcode) upon identification of a relocatable opcode, Bloomgren initiates a series of RISC instructions upon encountering an unsupported CISC instruction. As such, Bloomgren does not describe or suggest the subopcode detector recited in claim 6 and, accordingly, the rejection should be withdrawn.

Applicant submits that all claims are in condition for allowance.

Enclosed is a $420 check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 3/6/04

John F. Hayden
Reg. No. 37,640

Fish & Richardson P.C.
1425 K Street, N.W.
11th Floor
Washington, DC 20005-3500
Telephone: (202) 783-5070
Facsimile: (202) 783-2331

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